IN THE SPECIFICATION

Page 21, the first full paragraph, lines 3 to 13, replace the paragraph with:

On the other hand, the second semiconductor chip 2 is provided above the chip support surface 3a of the single-piece substrate 3, sandwiching the first semiconductor chip 1 in conjunction with the single-piece substrate 3. The first semiconductor chip 1 and the second semiconductor chip 2, which are provided above the chip support surface 3a of the single-piece substrate 3, are separated from each other by the die-bond film material 5 serving as an adhesive with the back surfaces 1c and ~~2a~~ 2c provided on the first semiconductor chip 1 and the second semiconductor chip 2 respectively facing the chip support surface 3a of the single-piece substrate 3.

Page 21, the second full paragraph, lines 14 to 23, replace the paragraph with:

That is, in the stack structure of the CSP 9, the first semiconductor chip 1 on the lower-layer side is connected as a flip chip to the single-piece substrate 3 in a phase-down mounting process. On the other hand, the second semiconductor chip 2 on the upper-layer side is wire-bonding connected to the back surface ~~1a~~ 1c provided on the first semiconductor

chip 1 in a phase-up mounting process. In this case, the thickness t2 of the second semiconductor chip 2 on the upper-layer side is made smaller than the thickness t1 of the first semiconductor chip 1 on the lower-layer side or $t1 \geq t2$ as shown in Fig. 2.

IN THE CLAIMS

Claims 1-7 (Withdrawn)

8. (Original) A semiconductor device manufacturing method comprising the steps of:

(a) preparing a wiring substrate having a plurality of electrodes created on a main surface thereof;

(b) preparing a first semiconductor chip having a main surface, a back surface, a plurality of semiconductor devices created on said main surface of said first semiconductor chip and a plurality of electrodes created on said main surface of said first semiconductor chip;

(c) preparing a second semiconductor chip having a main surface, a back surface, a plurality of semiconductor devices created on said main surface of said second semiconductor chip and a plurality of electrodes created on said main surface of said second semiconductor chip and having a thickness smaller than a thickness of said first semiconductor chip;

(d) placing said first semiconductor chip on said main surface of said wiring substrate with said main surface of said first semiconductor chip interfacing with said main surface of said wiring substrate in such a way that said

electrodes provided on said main surface of said first semiconductor chip interface with said respective electrodes provided on said main surface of said wiring substrate;

(e) after said step (d), applying a pressure to said back surface of said first semiconductor chip to electrically connect said electrodes provided on said first semiconductor chip to said respective electrodes provided on said wiring substrate;

(f) after said step (e), placing said second semiconductor chip on said back surface of said first semiconductor chip so as to make said back surface of said second semiconductor chip interface with said back surface of said first semiconductor chip through an adhesive by applying a pressure smaller than said pressure applied in said step (e);

(g) electrically connecting said electrodes created on said second semiconductor chip to said respective electrodes provided on said wiring substrate by using a plurality of wires; and

(h) forming a resin sealing body for sealing said first semiconductor chip, said second semiconductor chip and said wires.

9. (Original) A semiconductor device manufacturing method according to claim 8, wherein in said step (e), heat is applied to said first semiconductor chip at the same time as said applied pressure.

10. (Original) A semiconductor device manufacturing method according to claim 9, wherein said heat applied in said step (e) hardens the thermally-hardening resin placed between said main surface of said first semiconductor chip and said main surface of said wiring substrate, fixing said first semiconductor chip on said main surface of said wiring substrate through said the thermally hardening resin.

11. (Original) A semiconductor device manufacturing method according to claim 8, wherein in said step (e), a supersonic wave is radiated to said first semiconductor chip at the same time as said applied pressure.

12. (Original) A semiconductor device manufacturing method according to claim 11, wherein a metallic bump to serve as a protruding electrode is created on each of said electrodes provided on said first semiconductor chip and, in said step (e), a supersonic wave is radiated to said first

semiconductor chip at the same time as said applied pressure so as to take said first semiconductor chip into contact with said wiring substrate through ultrasonic metal-to-metal connection.

13. (Original) A semiconductor device manufacturing method according to claim 8, wherein said electrodes provided on said first semiconductor chip each comprise a pad created on said main surface of said first semiconductor chip and a protruding electrode placed on said pad.

14. (Original) A semiconductor device manufacturing method according to claim 8, further comprising, after said step (h), the step of creating a plurality of protruding electrodes created on a back surface of said wiring substrate, which are each used as an external electrode connected to a corresponding one of said electrodes provided on said main surface of said wiring surface.

15. (Original) A semiconductor device manufacturing method according to claim 8, further comprising, between said steps (e) and (f), the steps of:

(i) preparing a third semiconductor chip having a main surface, a back surface, a plurality of semiconductor devices created on said main surface and a plurality of electrodes created on said main surface;

(j) placing said third semiconductor chip on said main surface of said wiring substrate with said main surface of said third semiconductor chip interfacing with said main surface of said wiring substrate in such a way that said electrodes provided on said main surface of said third semiconductor chip interface with said respective electrodes provided on said main surface of said wiring substrate; and

(k) after said step (j), applying a pressure to said back surface of said third semiconductor chip to electrically connect said electrodes provided on said third semiconductor chip to said respective electrodes provided on said wiring substrate.

16. (Original) A semiconductor device manufacturing method according to claim 15, further comprising, after said step (k), the steps of:

(l) preparing a fourth semiconductor chip having a main surface, a back surface, a plurality of semiconductor devices created on said main surface and a plurality of electrodes

created on said main surface and having a thickness smaller than a thickness of said third semiconductor chip;

(m) placing said fourth semiconductor chip on said back surface of said third semiconductor chip so as to make said back surface of said fourth semiconductor chip interface with said back surface of said third semiconductor chip through an adhesive by applying a pressure smaller than said pressure applied in said step (k); and

(n) electrically connecting said electrodes created on said fourth semiconductor chip to said respective electrodes provided on said wiring substrate by using a plurality of wires.

17. (Currently Amended) A semiconductor device manufacturing method comprising the steps of:

(a) preparing a mold provided with a cavity having first and second side surfaces facing each other and third and fourth surfaces facing each other and coming in contact with said first and second side surfaces and provided with a resin injection entrance created on said first side surface;

(b) preparing a wiring substrate having a main surface, preparing a first semiconductor chip fixed on said main

surface of said wiring substrate and preparing a second semiconductor chip fixed on said first semiconductor chip;

(c) placing said wiring substrate, said first semiconductor chip and said second semiconductor chip inside said cavity; and

(d) after said step (c) injecting resin through said resin injection entrance in order to seal and hold said first and second semiconductor chips,

wherein in said step (c), said wiring substrate, said first semiconductor chip and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said third side surface of said cavity, the length of said first semiconductor chip exceeds the length of said second semiconductor chip, and

wherein in said step (c), said wiring substrate, said first semiconductor chip, and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said first side surface of said cavity, the length of said first semiconductor chip is smaller than the length of said second semiconductor chip.

Claim 18 (Canceled)

19. (Original) A semiconductor device manufacturing method according to claim 17, wherein said mold has an air hole created on said second side surface of said cavity.

20. (Currently Amended) A semiconductor device manufacturing method comprising the steps of:

(a) preparing a mold provided with a cavity having first and second side surfaces facing each other and third and fourth surfaces facing each other and coming in contact with said first and second side surfaces and provided with a plurality of resin injection entrances created on said first side surface;

(b) preparing a wiring substrate having a main surface and a plurality of device areas created thereon, preparing a first semiconductor chip fixed on each of said device areas of said wiring substrate and preparing a second semiconductor chip fixed on each of said first semiconductor chips;

(c) placing said wiring substrate, said first semiconductor chips and said second semiconductor chips inside said cavity, and then collectively cover said device areas by using said cavity; and

after said step (c), injecting resin through said resin injection entrances associated with said device areas in order

to collectively seal and hold said first and second semiconductor chips,

wherein in said step (c), said wiring substrate, said first semiconductor ~~chip~~ chips and said second semiconductor ~~chip~~ chips are arranged in such a way that, on a cross section parallel to said third side surface of said cavity, said length of each of said first semiconductor chips exceeds said length of ~~said~~ corresponding second semiconductor ~~chip~~ chips stacked on said first semiconductor ~~chip~~ chips, and

wherein in said step (c), said wiring substrate, said first semiconductor chips, and said second semiconductor chips are arranged in such a way that, on a cross section parallel to said first side surface of said cavity, the length of each of said first semiconductor chips are smaller than the length of corresponding second semiconductor chips stacked on said first semiconductor chips.

Claims 21-43 (Withdrawn)

REMARKS

Applicants request reconsideration of the rejection.

Claims 8-17 and 19-20 are under examination, claims 1-7 and 21-43 having been withdrawn and claim 18 being canceled in this Paper.

Submitted herewith are certified copies of the corresponding Japanese patent applications (JP 2002-012775, filed January 22, 2002 and JP 2001-108603, filed April 6, 2001). An indication that these documents have been safely received would be appreciated.

Claims 8, 14, 15, and 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al JP 2000-188369 (Hiroyuki) in view of Takiar et al U.S. Patent No. 5,422,435 (Takiar). The Applicants request reconsideration as follows.

Claim 8 is directed to a semiconductor device manufacturing method, and includes among its steps a step (e) of applying a pressure to the back surface of the first semiconductor chip to electrically connect the electrodes provided on the first semiconductor chip to the respective electrodes provided on the wiring substrate on which the first semiconductor chip is placed. Recognizing that the primary reference to Hiroyuki fails to teach the application of

pressure to the first semiconductor chip so as to electrically connect it to the electrodes of the wiring substrate, the Examiner cites Takiar as teaching this feature in column 10, lines 34+, with additional reference to figure 5.

However, reference to this passage and figure of Takiar shows no description of the electrically connecting step required by claim 8. This step, referred to in the specification as "pressure welding" (for example, page 20, lines 14-21) is characteristic of the claimed method in which the first semiconductor chip is flip-chip mounted. In the prior art, there has been a problem of chip cracking under the load of mounting the semiconductor chips, and the prior art has thickened the semiconductor chips to prevent the chip cracking. However, thicker semiconductor chips lead to larger packages, which is less desirable in the art. In combination with the other steps of claim 8, the pressure welding described in step (e) achieves a flip-chip mounted semiconductor chip in a semiconductor package manufactured according to the claimed method, which overcomes problems of the prior art.

In column 10, lines 34-39, Takiar teaches to apply an adhesive or soft-solder 48 onto the principal mounting surface 40 of a carrier member 42, followed by dispensing a

semiconductor die 22 onto the adhesive 48. As shown in figure 5, semiconductor die 146 (corresponding to semiconductor die 22) is electrically connected to carrier member 152 (corresponding to carrier member 42) by wire bonding. Furthermore, although the patent states that "the choice of die or substrate, as well as the particular wire bonding interconnections to be made, depends upon the particular application for which the multi-chip module is to be used" (column 8, lines 44-47), the patent does not disclose or suggest the claimed pressure welding as an alternative to wire bonding of the first semiconductor chip. Therefore, even in combination with Hiroyuki, Takiar does not teach the claimed invention.

Claims 9 and 10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al JP 2000-188369 (Hiroyuki) in view of Takiar et al U.S. Patent No. 5,422,435 (Takiar) and in further view of Lau, Flip Chip Technologies 1996 (McGraw-Hill, p. 302-303) (Lau). Claims 11, 12, and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al JP 2000-188369 (Hiroyuki) in view of Takiar et al U.S. Patent No. 5,422,435 (Takiar) and in further view of Okazaki et al U.S. Patent No. 6,269,999. Claims 9-13

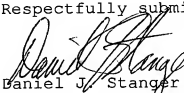
are dependent from claim 8, and thus inherit its patentability as discussed above.

Claims 17 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al JP 2000-188369 (Hiroyuki). The subject matter of claim 18 has been added to independent claim 17, rendering it patentable (claim 18 does not stand rejected). Because claim 19 is dependent from the amended claim 17, claim 19 is also patentable.

Claim 20 was rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al JP 2000-188369 (Hiroyuki) in view of Mitsuhiro JP 03-106622 (Mitsuhiro). The subject matter of claim 18 (patentable as noted above) has also been added to independent claim 20, thus rendering it patentable as well.

In view of the foregoing amendments and remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



Daniel J. Stanger
Registration No. 32,846
Attorney for Applicant(s)

MATTINGLY, STANGER & MALUR, P.C.
1800 Diagonal Road, Suite 370
Alexandria, Virginia 22314
Telephone: (703) 684-1120
Facsimile: (703) 684-1157
Date: August 18, 2003